

# Vertex Detector Options and R&D Requirements

Upgrade DC Meeting

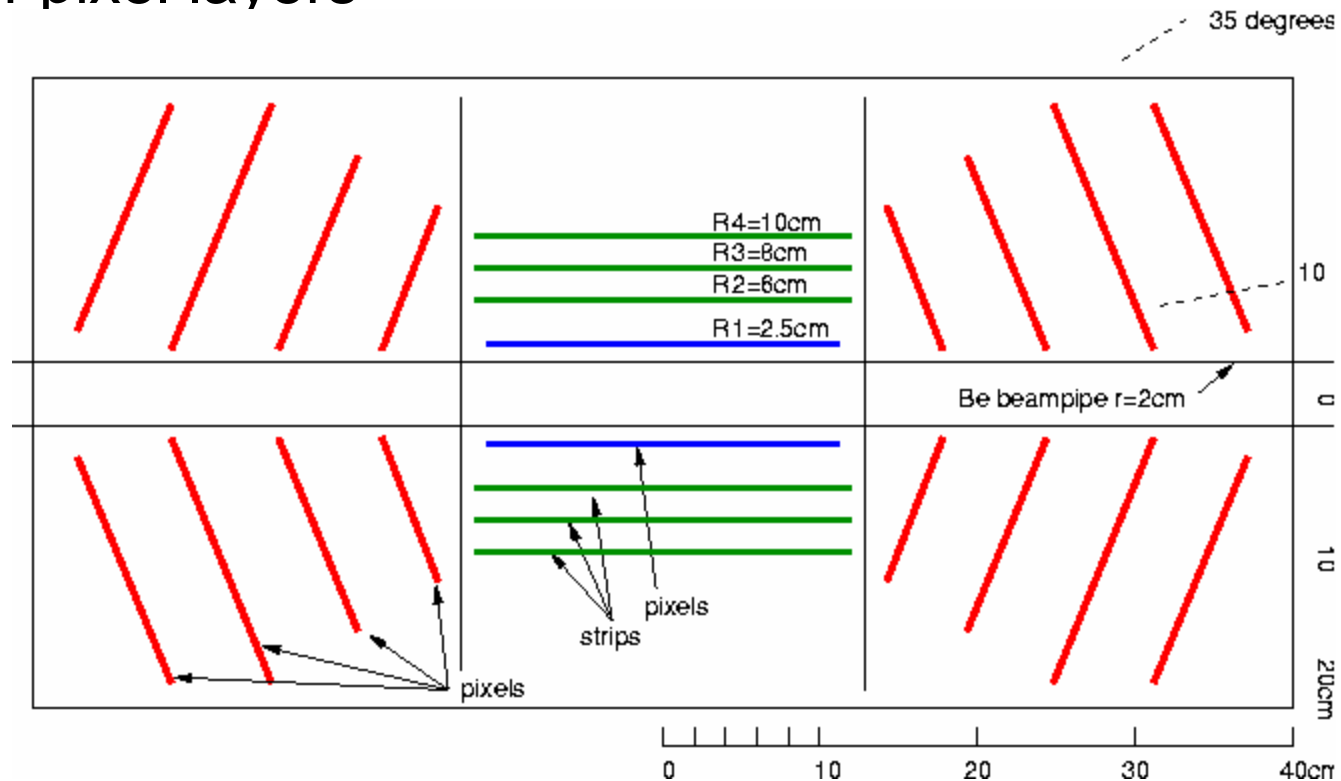
December 11, 2002

Yuji Goto (RIKEN/RBRC)

for the Silicon USG

# Strawman design

- Barrel
  - 1 pixel layer and 3 strip layers
- Endcap
  - 4 pixel layers



# Strawman design

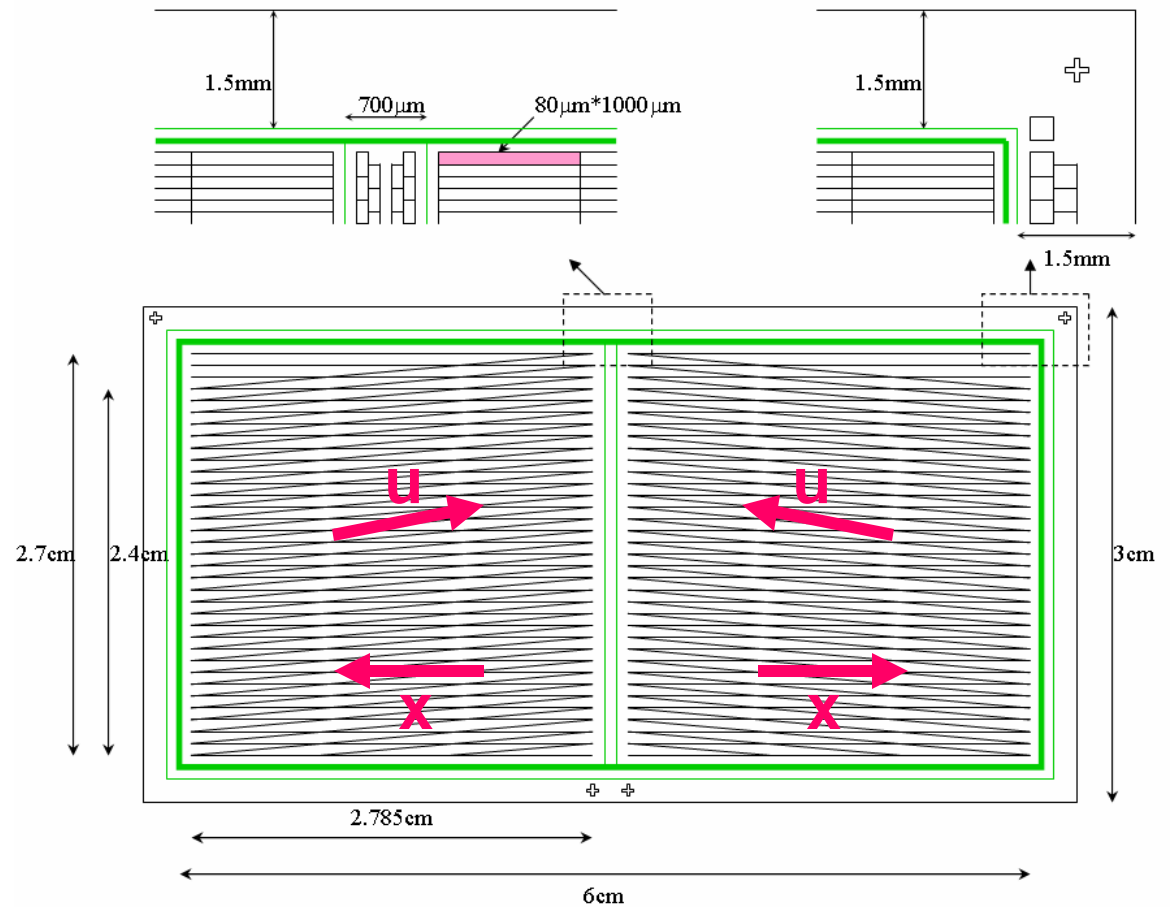
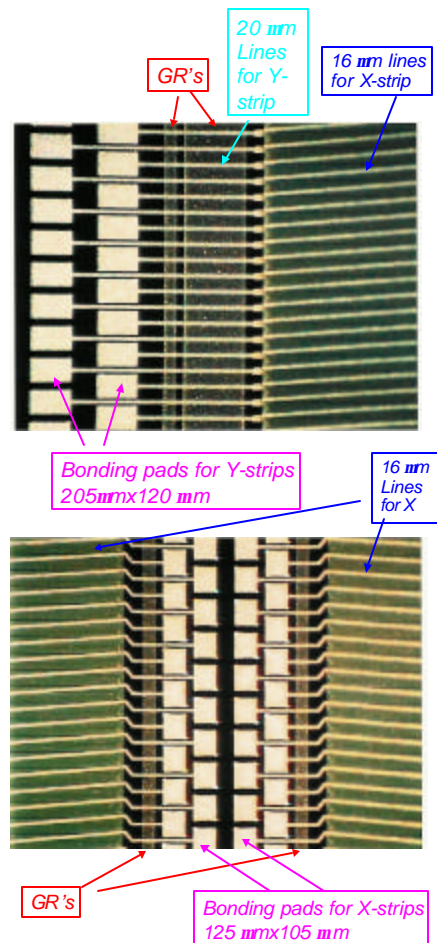
- Barrel
  - 1<sup>st</sup> pixel layer
    - $r=2\text{cm}$ ,  $|z|<11.2\text{cm}$
    - 1.3M channel = 1.3Mbit for 1-bit (binary) readout
  - 2<sup>nd</sup>-4<sup>th</sup> strip layers
    - $r=6, 8, 10\text{cm}$ ,  $|z|<15\text{cm}$
    - 360K channel = 2.9Mbit for 8-bit readout

## R&D Items

- Strip sensor
- Strip readout / Interface with PHENIX
- Hybrid pixel
- Hybrid pixel readout / Interface with PHENIX
- Endcap hybrid pixel
- Bump bonding / Thinning
- Monolithic pixel
- Support frame

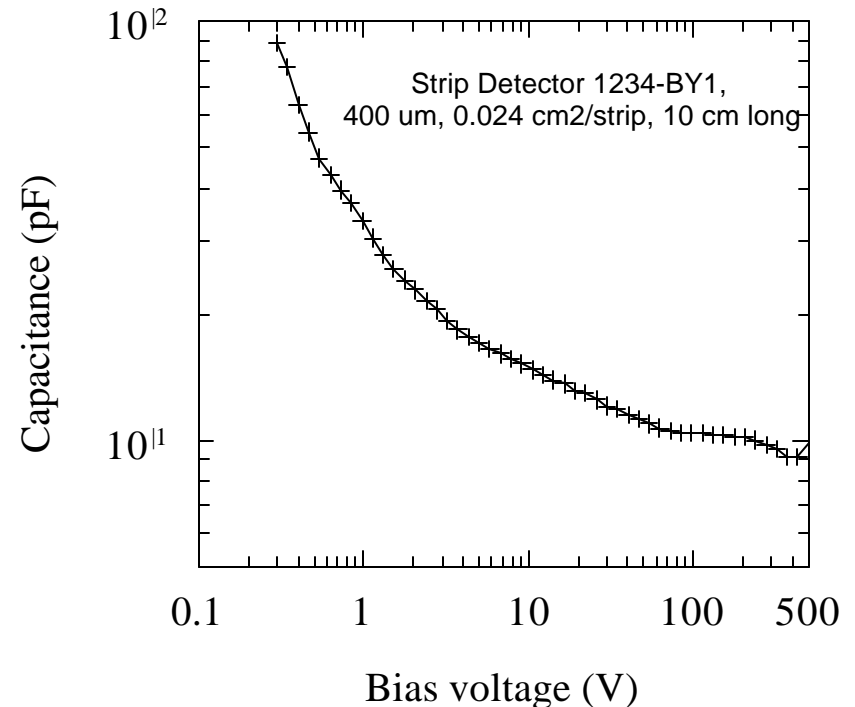
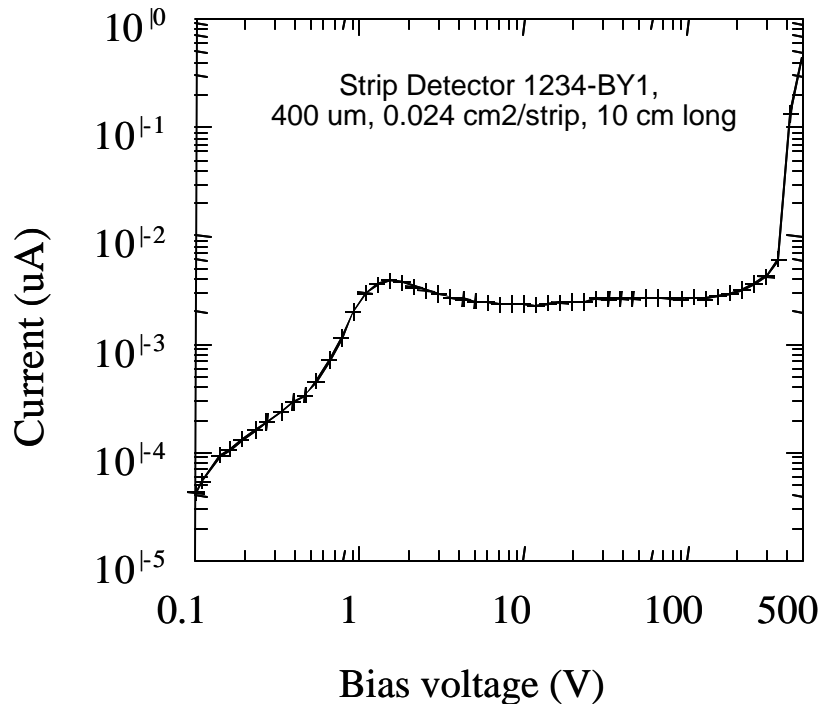
# Strip sensor

- Sensor by Zheng Li (BNL instr. div.)



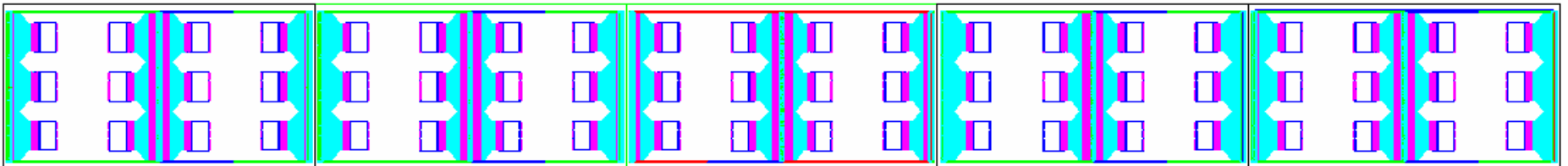
# Strip sensor

- Sensor by Zheng Li (BNL instr. div.)
  - DC coupling
  - full depletion at  $\sim 80$  V – capacitance  $\sim 10$  pF
  - leakage current  $\sim 10$  nA



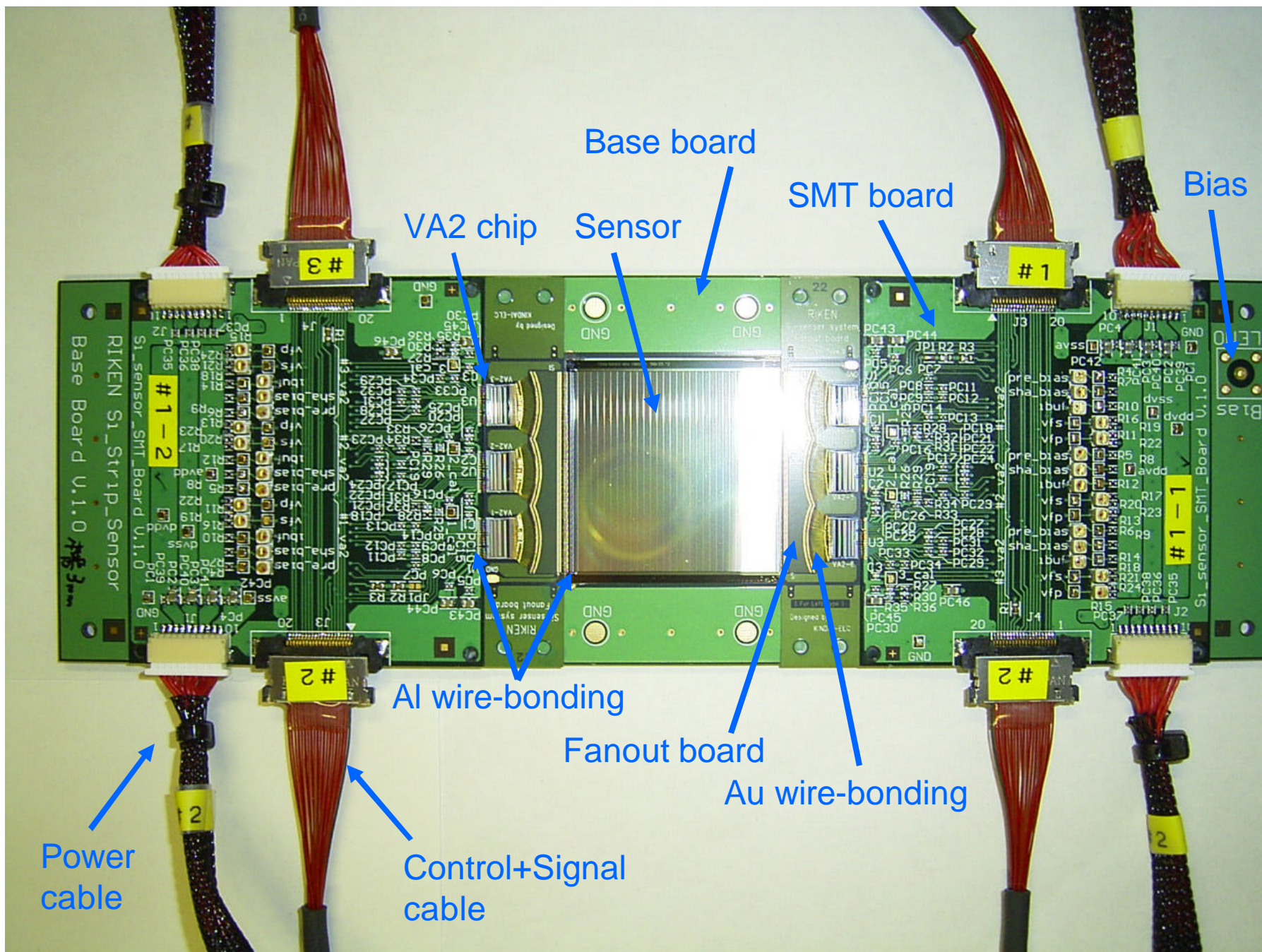
# Strip sensor

- Ladder structure
  - 5 sensors / ladder
  - 12 readout chips / sensor
    - SVX4 or TGV+AMU/ADC
  - cooling
    - SVX4:  $3.5 \text{ mW/ch} \times 360 \text{ Kch} = 1.3 \text{ KW}$
    - SVX4: necessary to decrease leakage current ...
  - cabling
    - Cu (Al) / Polyimide hybrid for low material budget
  - ladder material
    - e.g. CFRP



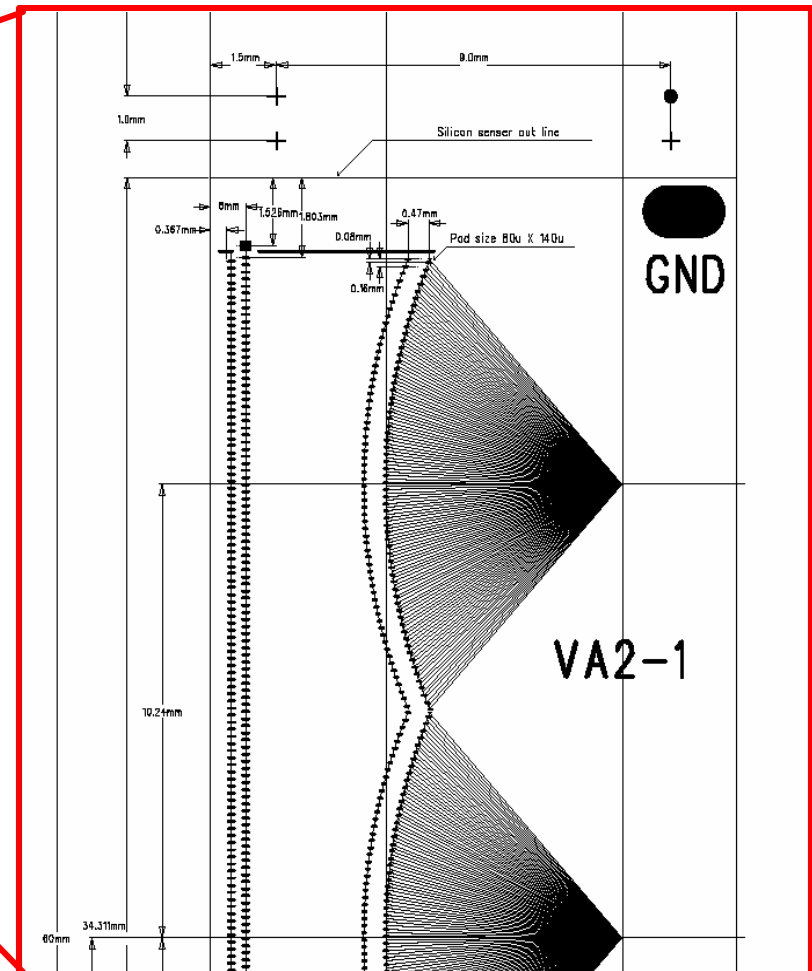
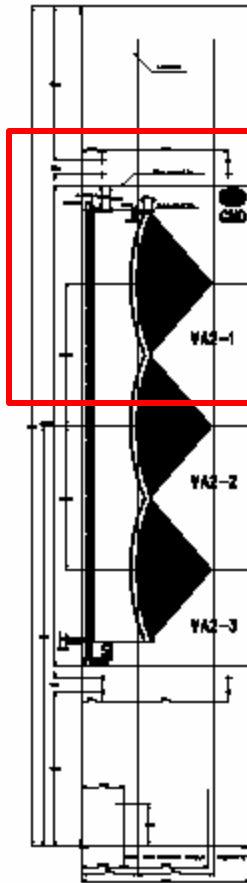
# Strip sensor

- Status
  - 400  $\mu\text{m}$  thickness and 250  $\mu\text{m}$  thickness
  - wire-bonding (of both Al and Au)
  - glues between the sensor and the base board
  - leakage current
  - VA2 readout chip operation
  - test beam at KEK
    - position resolution
    - detection efficiency
    - charge correlation property
    - two track separation efficiency



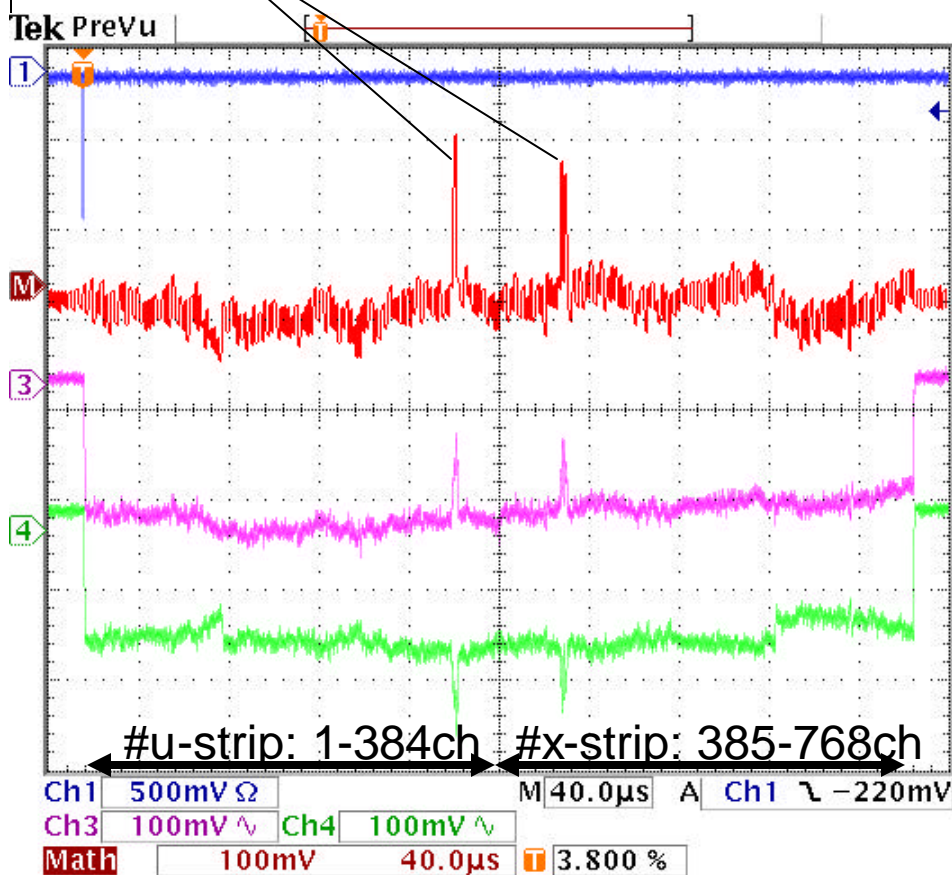
# Strip sensor

- Fanout



# Strip sensor

Cosmic ray signal



Ch1: Trigger w/ Scinti's

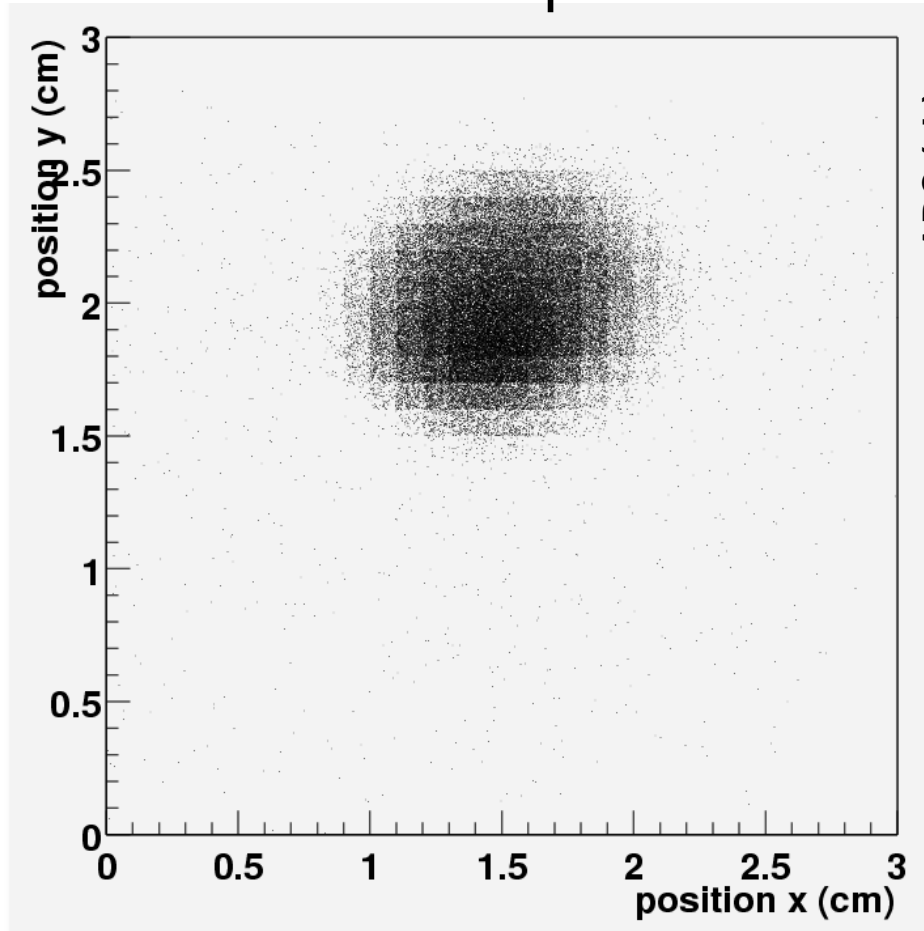
ChM: Ch3-Ch4

Ch3: Analog pos.

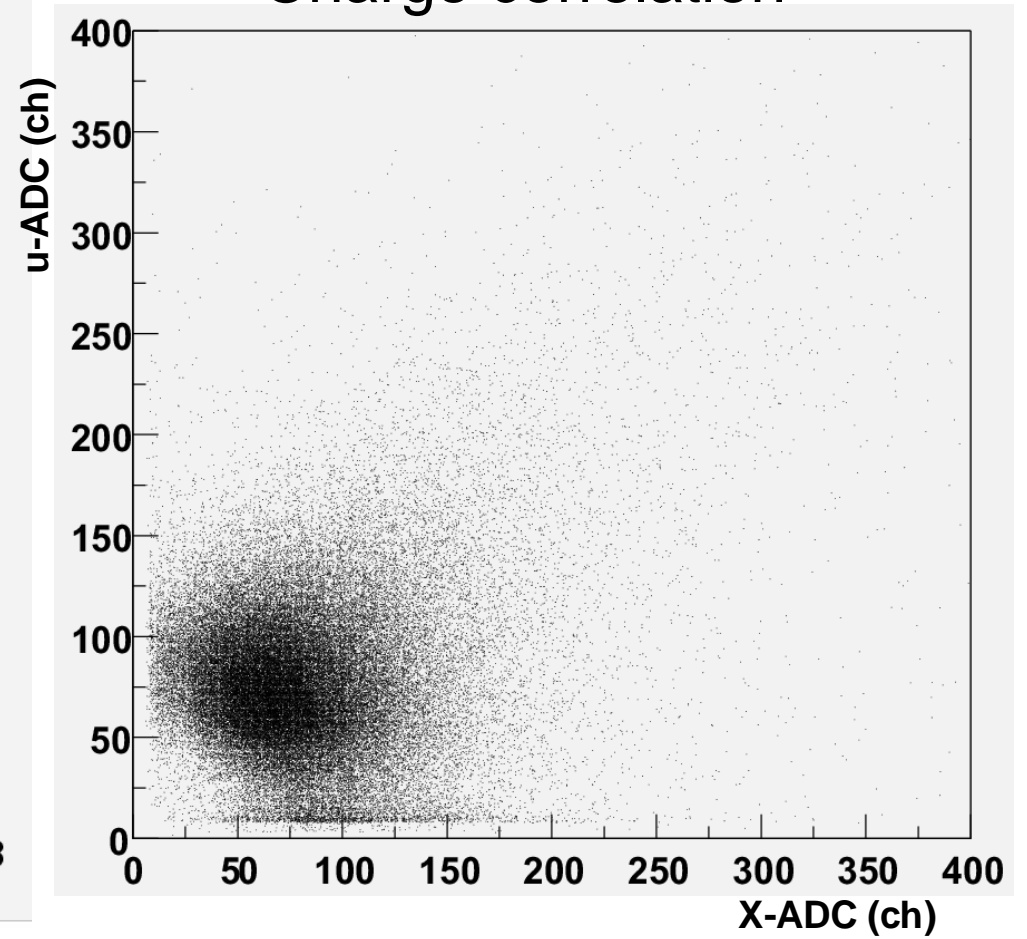
Ch4: Analog neg.

# Strip sensor

Measured position



Charge correlation



# Strip sensor readout / Interface with PHENIX

- Technical options
  - SVX4 chip (preamp + digitized pipeline)
    - AC coupling
      - must take care of accumulated leakage current
      - by frequent reset ? (at the abort gap ?)
      - operation temperature lower than the room temperature ?
  - TGV preamp + AMU/ADC
    - DC coupling
    - output drive capability ?
      - local processing or driving the preamp signals on kapton cables
  - readout time ?
  - buffering capability ?

# Strip sensor readout / Interface with PHENIX

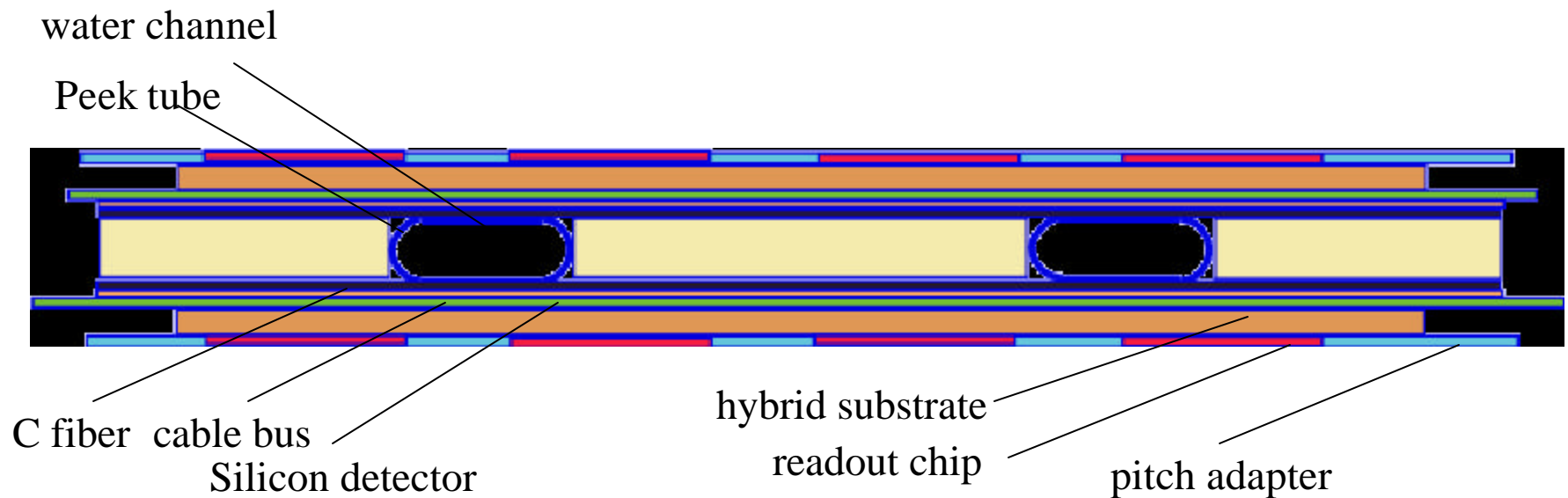
- Technical options
  - data management ?
    - FPGA (rad-hard ?) or digital-ASIC ?
    - low power data transmission that avoid using G-Links
- R&D
  - design concept
  - data transmission to the DCM
  - list of parts
  - build and test a prototype

# Strip sensor readout / Interface with PHENIX

- Schedule / Manpower
  - design concept in FY2003
  - ORNL internal funding ?
- Milestones / Decision points
  - secure funding
  - data management and transmission
  - design completion
  - prototype construction
  - prototype testing

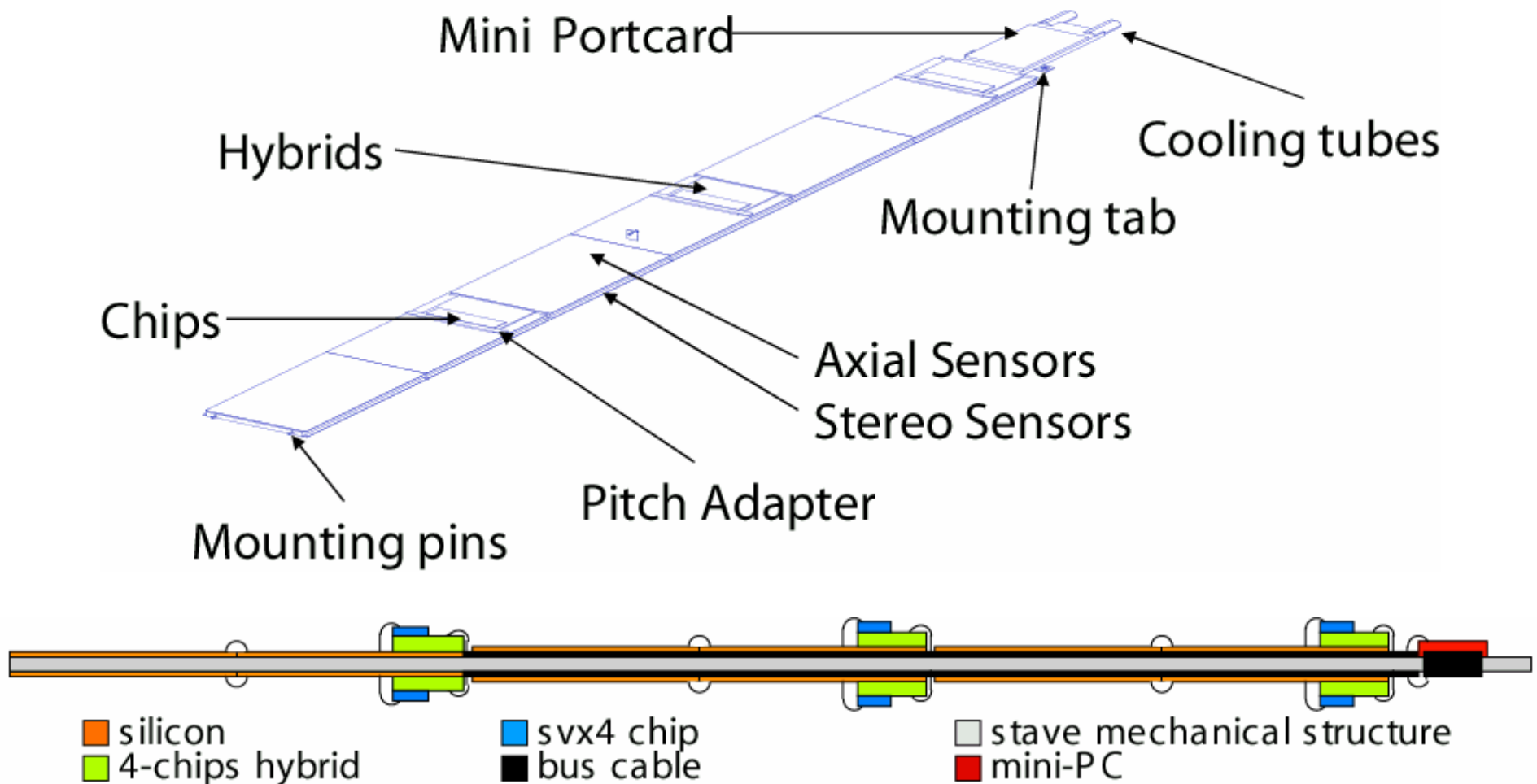
# CDF-II silicon upgrade for Run-IIB

- Stave
  - $\sim 1.5\%$  radiation length per stave



# CDF-II silicon upgrade for Run-IIB

## Run IIB Stave



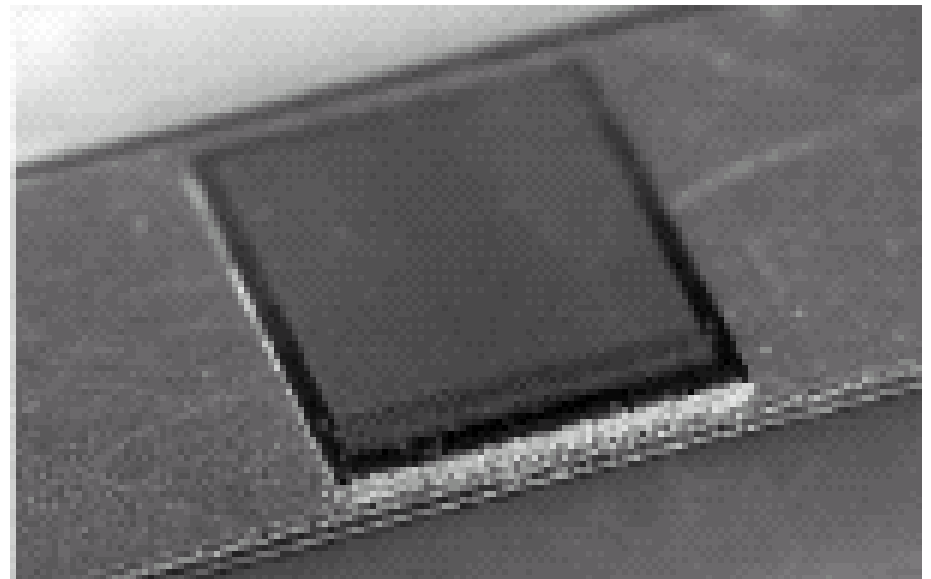
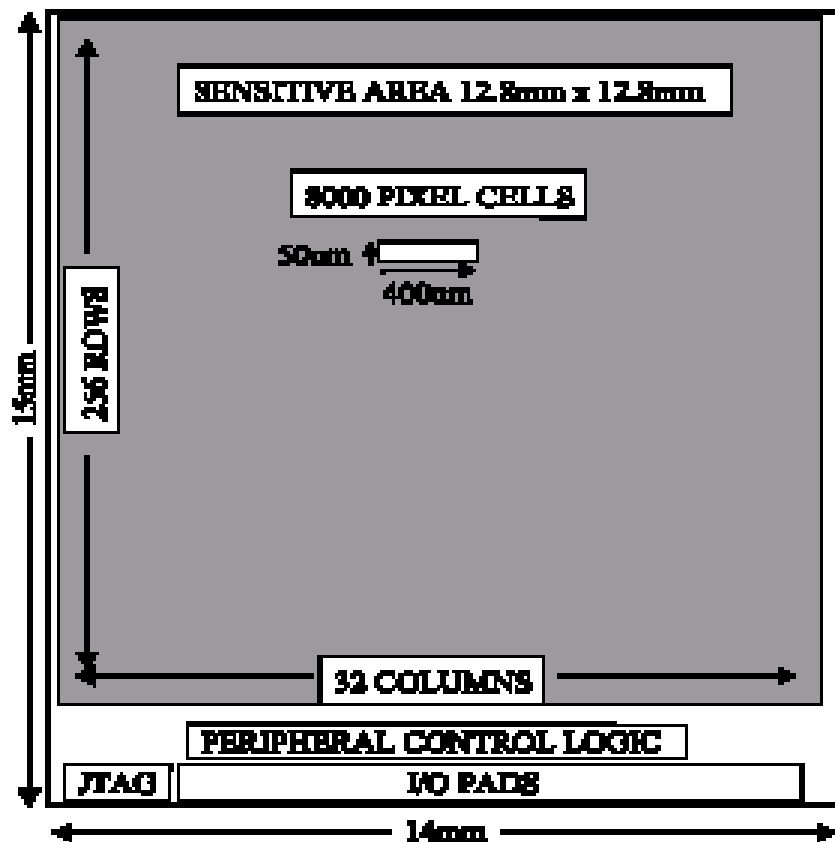
# CDF-II silicon upgrade for Run-IIB

- Port card



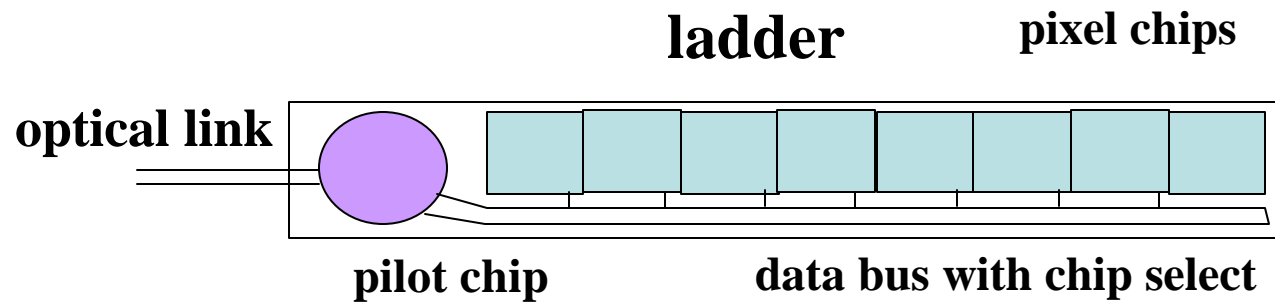
# Hybrid pixel

- ALICE1 chip
  - 32 x 256 pixels of 425 mm (z) x 50 mm (rf)
  - size: 13.6 mm x 15.95 mm

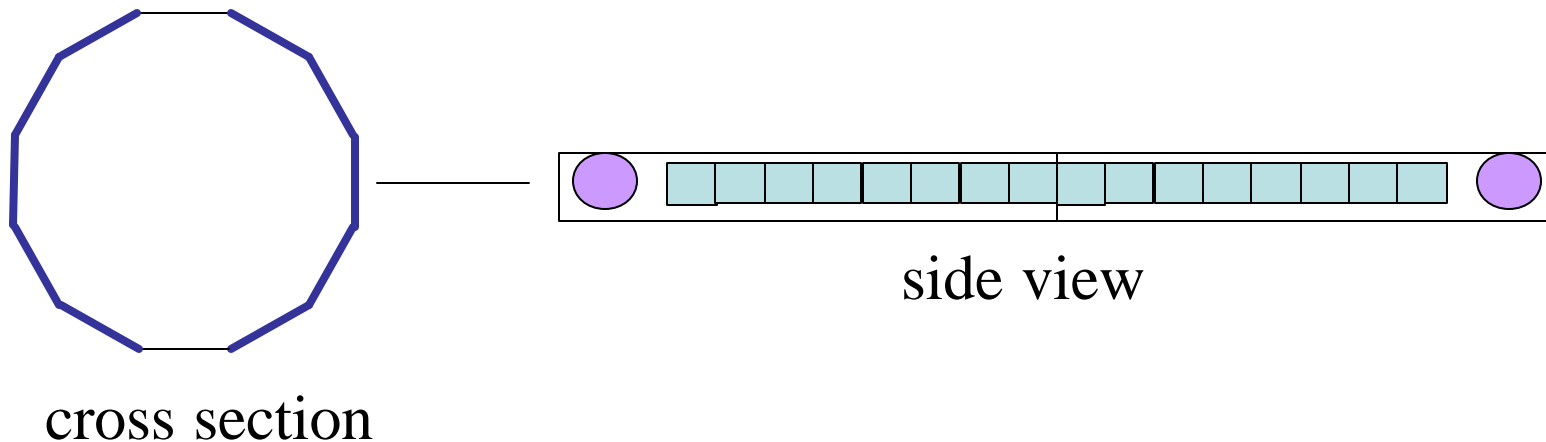


# Hybrid pixel

- Ladder structure
  - 8 chips/ladder + 1 pilot



- 20 ladders for 1<sup>st</sup> layer
  - $8192 \times 8 \times 20 = 1.3 \text{ Mchannel}$

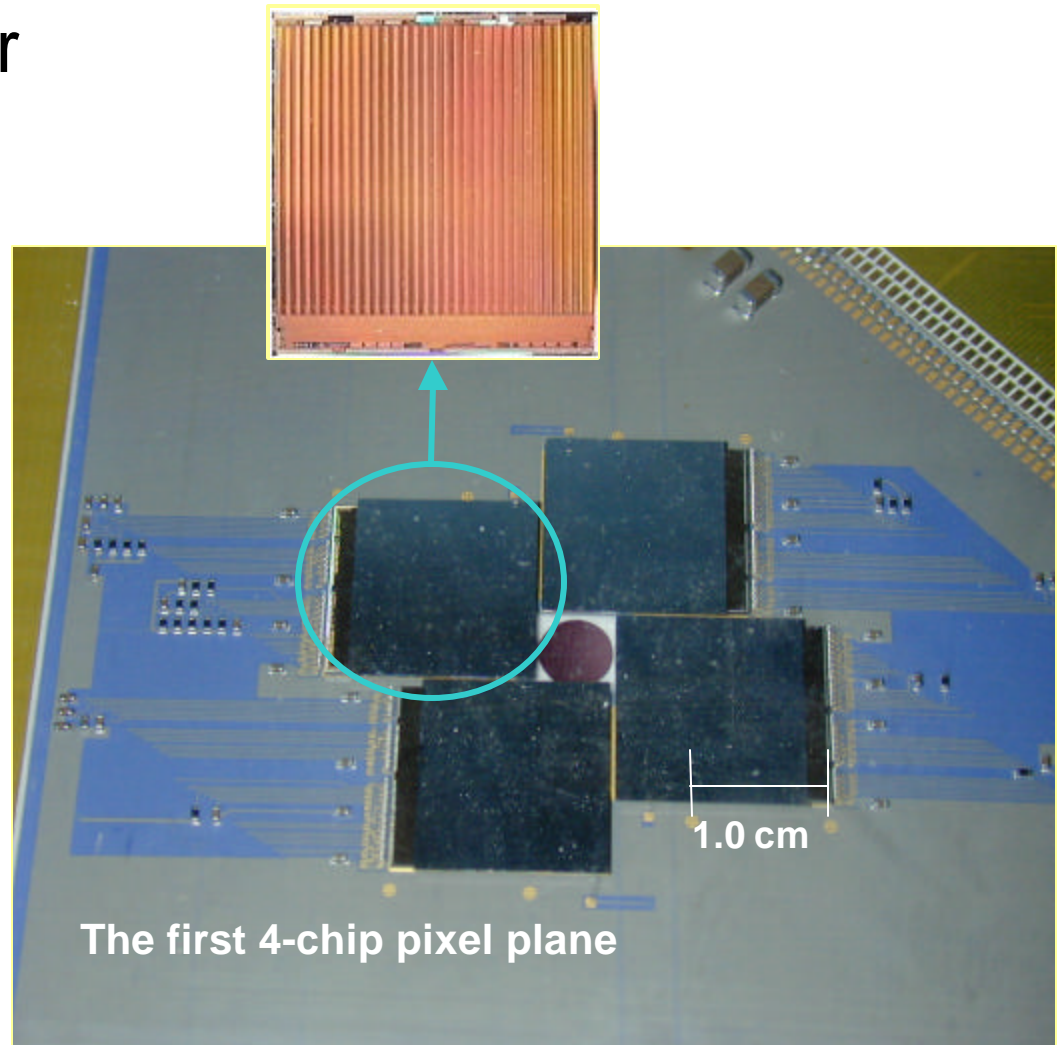
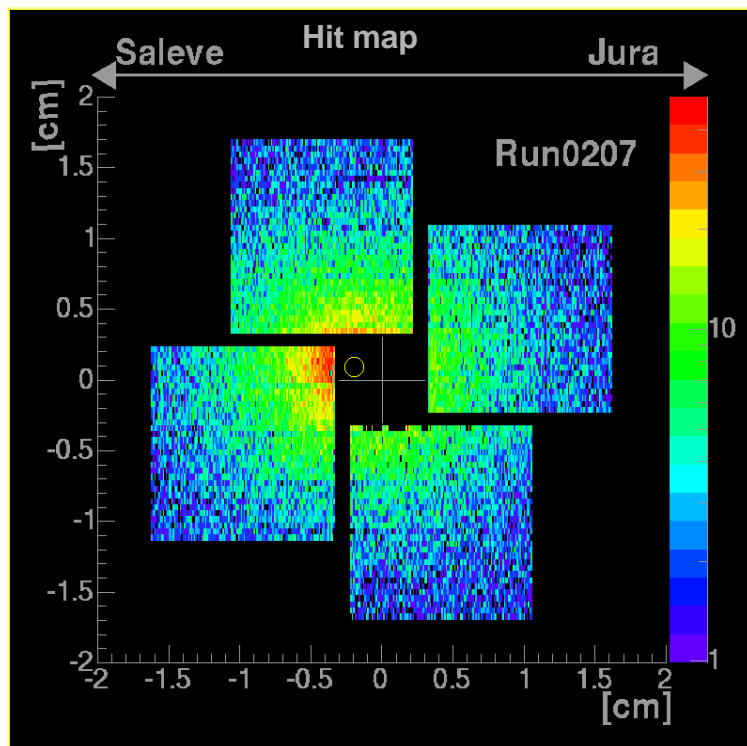


# Hybrid pixel

- NA60 pixel detector
  - pixel detector developed at CERN for application in ALICE and LHCb
  - ALICE1LHCb chip: 8192 pixels of  $50\text{ }\mu\text{m} \times 425\text{ }\mu\text{m}$ , radiation hard
  - 16 NA60 specific 4- and 8-chip planes, 10 MHz clk, 200 ns strobe
  - PCI readout by NA60
  - Linux based DAQ

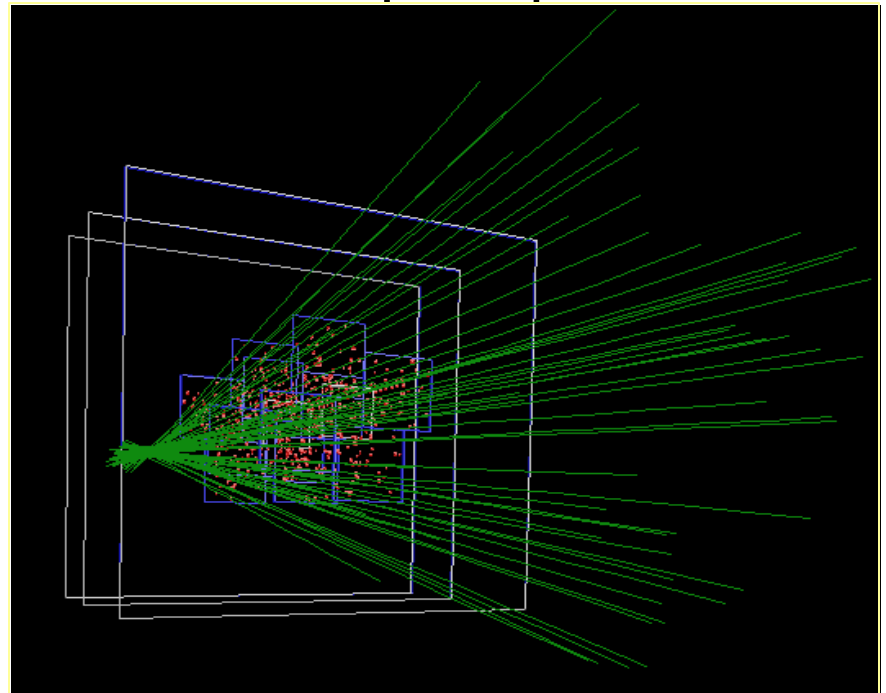
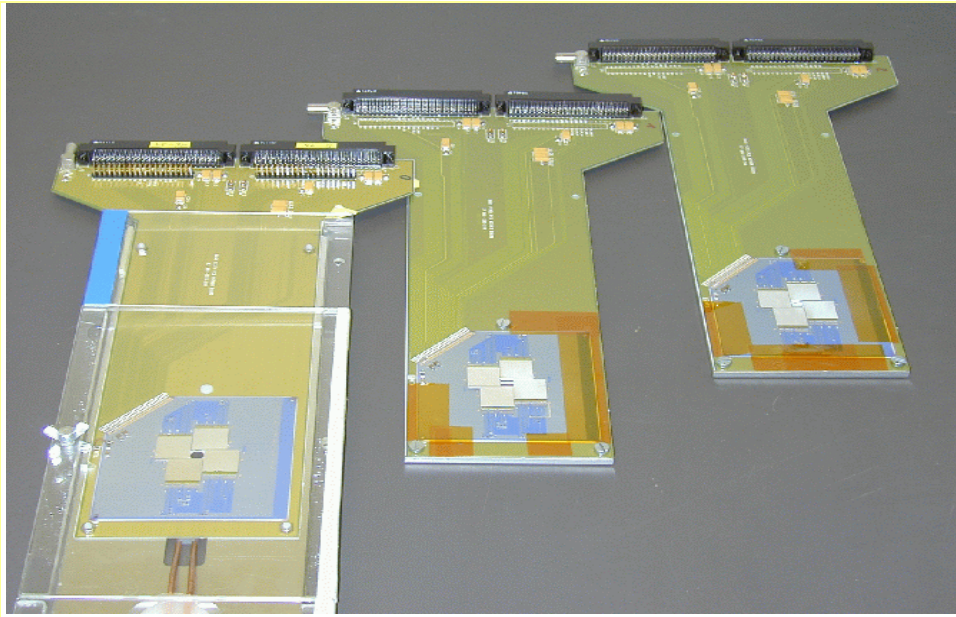
# Hybrid pixel

- NA60 pixel detector



# Hybrid pixel

- NA60 pixel detector
  - first three 4-chip pixel planes constructed
  - test of vertex spectrometer with 20 and 30 GeV/c Pb beams on Pb targets, preparing for physics run in 2003
  - tracking and vertex reconstruction with pixel planes



# Hybrid pixel readout

- ALICE1 chip readout
  - 32 parallel lines, each reads 256 channels serially
  - readout speed: 10 MHz  $\rightarrow$  25.6  $\mu$ s/chip
  - data buffer for 4 events
    - PHENIX standard – 5 events
  - no data format (header, footer, parity bits, ...)
  - no zero-suppression
    - must be taken care at somewhere (pilot, FEM, or DCM ?)
  - L1 trigger be in timing – 5.5  $\mu$ sec in ALICE
    - 4  $\mu$ sec in PHENIX – OK

# Hybrid pixel readout

- ALICE pilot chip multi-chip module (PCMCM)
  - readout 10 chips serially  $\rightarrow$  256  $\mu$ s/event in ALICE
    - must 40 or 80  $\mu$ s/event in PHENIX
  - slow control (via JTAG)
- R&D
  - parallelize readout ?
    - 2 or more pilot chips in a ladder
    - sequential parallel readout
    - ...
  - development of our own pilot chip and/or other FEMs
    - KEK experts are interested in the development
    - data bus is a critical issue

# Hybrid pixel readout / Interface with PHENIX

- FEM for hybrid pixel readout
  - data receiver from pixel detector
  - data processor
    - FPGA for flexible data compression and data formatting ?
  - data transmitter to the DCM
  - slow controller for setup and monitoring of the pixel detectors
    - CCB (central control board) to separate the slow control ?
- FEM for strip readout ?
  - same FEM, different receiver

# Hybrid pixel readout / Interface with PHENIX

- R&D
  - FPGA code development with a programmable fake data source
    - readout with the DC-FEM DAQ chain
    - zero-suppression at the FEM ?
  - transmitter / receiver interface
  - fake source → ALICE pixel prototype
    - slow control system to be integrated in the PHENIX framework
    - slow control at CCB ?
  - prototype boards of FEM and CCB

# Hybrid pixel readout / Interface with PHENIX

- Schedule / Manpower
  - all decisions by end of FY2004
    - 2 MSI students
    - 1 postdoc (1/2 by DOE fund)
    - 1/4 electrical engineer (by DOE fund)

# Hybrid pixel readout / Interface with PHENIX

- Milestones

- FY2003

- define pixel-FEM and FEM-DCM interface
    - evaluate use pixel FEM for other PHENIX silicon detectors
    - readout fake data source by DC FEM to DCM
    - develop data processor FPGA code for zero-suppression
    - obtain ALICE pixel prototype
    - implement interface and readout single ALICE pixel-chip
    - adapt slow control to PHENIX framework

- FY2004

- design readout system for central pixel barrel
    - decide to build separate CCB or incorporate into FEM
    - prototype PHENIX pixel FEM (and CCB)
    - test multi pixel-chip ladder with PHENIX FEM (and CCB) prototype

# Endcap hybrid pixel

- Plan
  - utilize the same sensor technology and the same chip that is used for the barrel hybrid pixel
  - change the topology to match the endcap requirements
- Issues
  - increased capacitance load on the readout chip
  - sensor pad topology
  - routing of control lines
  - location of the pilot chip

## Endcap hybrid pixel

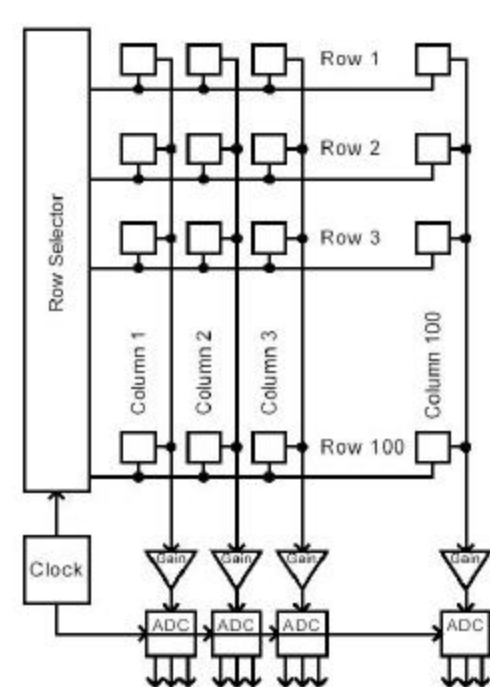
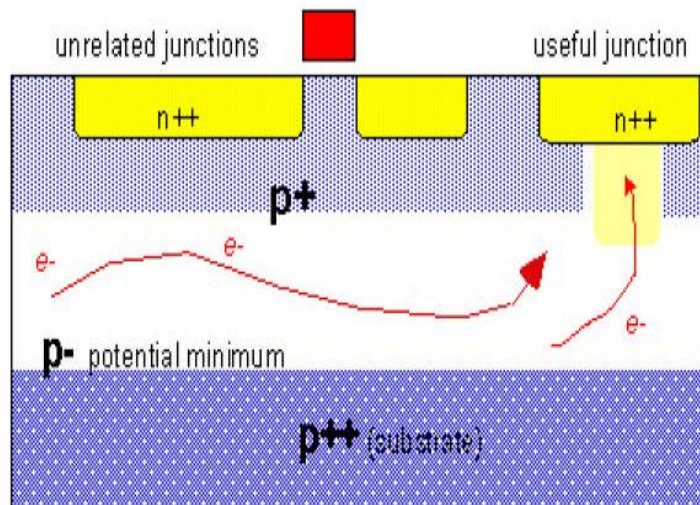
- **Schedule / Manpower**
  - begin design modifications in FY2004
  - finish prototyping in FY2005
  - who and where ? – answers by the review ...
- **Milestones**
  - define the technology by the review next year
  - complete prototyping by the middle of FY2005

# Bump bonding / Thinning

- Technical options
  - FNAL-led efforts
    - McNC North Carolina / Unitive
    - AIT Hong-Kong
  - CERN-led efforts
    - IZM Berlin
    - VTT Finland

# Monolithic pixel

- Technical options
  - epitaxial monolithic detectors by LEPSI
  - float-zone monolithic detectors by Bonn and Munich



# Support frame

- Technical options
  - conceptual design by the engineering team that designed the ATLAS support frame (HYTEC)
  - recommendation as to the best technical approach and the areas that need further study and prototyping
- Schedule
  - conceptual design complete in mid FY2003
    - model concept by the review ... (not the final)
  - R&D and prototyping finished by mid FY2005

# Support frame

- Mockup of the barrel support structure
  - made by CFPR
  - Precision, strength, deformation and material budget to be measured

